1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS successive approximation 12-bit analog-to-digital converter allowing unipolar or bipolar input ranges and converting in 5 or 10 μs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD7672T(X)05/883B and AD7672T(X)10/883B
−2	AD7672U(X)05/883B and AD7672U(X)10/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C)

V_{DD} to DGND ..... −0.3 V, +7 V
V_{SS} to DGND ..... +0.3 V, −17 V
AGND to DGND ..... −0.3 V, V_{DD} +0.3 V
AIN1, AIN2 to AGND ..... −15 V, +15 V
V_{REF} to AGND ..... V_{SS} −0.3 V, V_{DD} +0.3 V
Digital Input Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
Digital Output Voltage to DGND ..... −0.3 V, V_{DD} +0.3 V
Power Dissipation (to +75°C) ..... 450 mW
Derates above +75°C ..... 6 mW/°C
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

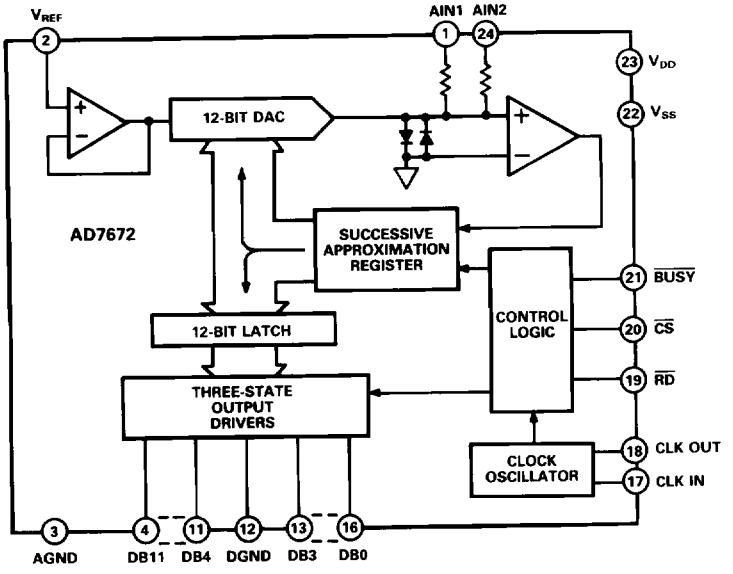
AD7672—SPECIFICATIONS

Table 1.

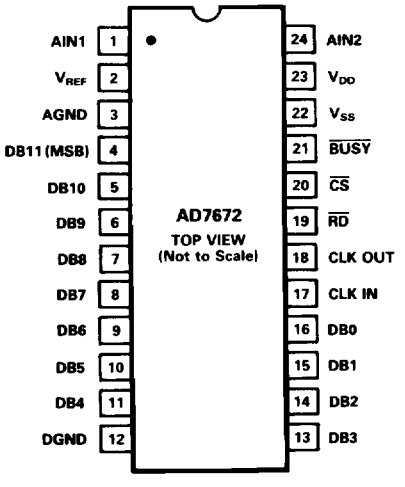
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2	12				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	−1	1	1	1		Tested Range ±5 V	±LSB max
		−2	3/4	1	3/4	1/2		
Differential Nonlinearity	DNL	−1, 2	0.9	0.9	0.9			±LSB max
Unipolar Offset Error		−1	6	5	6		Input Range 0 to 5 V or 0 to 10 V	±LSB max
		−2	4	5	4	3		
Unipolar Gain Error		−1	7	5	7		Input Range 0 to 5 V or 0 to 10 V	±LSB max
		−2	6	5	6	4		
Bipolar Zero Error		−1	6	5	6		Input Range ± 5 V	±LSB max
		−2	4	5	4	3		
Bipolar Gain Error		−1	7	5	7		Input Range ± 5 V	±LSB max
		−2	6	5	6	4		
Unipolar Input Current		−1, 2	3.5	3.5	3.5		Input Range: 0 to 5 V or 0 to 10 V	mA max
Bipolar Input Current		−1, 2	1.75	1.75	1.75		Input Range: ±5 V	±mA max
Reference Input Current		−1, 2	−3					μA max
Digital Input Low Level	V_{IL}	−1, 2	0.8	0.8	0.8		$\overline{CS}$, $\overline{RD}$, CLK IN	V max
Digital Input High Level	V_{IM}	−1, 2	2.4	2.4	2.4		$\overline{CS}$, $\overline{RD}$, CLK IN	V min
Digital Input Capacitance	C_{IN}	−1, 2	10				$\overline{CS}$, $\overline{RD}$, CLK IN	pF max
Digital Input Current (1)	I_{I1}	−1, 2	±10	±10	±10		$\overline{CS}$, $\overline{RD}$, V_{IN} = 0 to V_{DD}	±μA max
Digital Input Current (2)	I_{I2}	−1, 2	±20	±20	±20		CLK IN, V_{IN} = 0 to V_{DD}	±μA max
Digital Output Low Level	V_{OL}	−1, 2	0.4	0.4	0.4		DB11–DB0, $\overline{BUSY}$, CLK OUT	V max
Digital Output High Level	V_{OH}	−1, 2	4.0	4.0	4.0		DB11–DB0, $\overline{BUSY}$, CLK OUT	V min
Floating State Leakage Current	I_{OUT}	−1, 2	±10	±10	±10		DB1–DB0	±μA max
Floating State Output Capacitance	C_{OUT}	−1, 2	15					pF max
Conversion Time[2] Synchronous Clock	t_{CONV}	−1, 2	5	5	5		f_{CLK} = 2.5 MHz	μs max
			10	10	10		f_{CLK} = 1.25 MHz	
Conversion Time[2] Asynchronous Clock	t_{CONV}	−1, 2	4.8	4.8	4.8		f_{CLK} = 2.5 MHz	μs min
			5.2	5.2	5.2			μs max
Conversion Time[2] Asynchronous Clock	t_{CONV}	−1, 2	9.6	9.6	9.6		f_{CLK} = 1.25 MHz	μs min
			10.4	10.4	10.4			μs max
Supply Current from V_{SS}	I_{SS}	−1, 2	−12	−12	−12		$\overline{CS}$ = $\overline{RD}$ = V_{DD} AIN1 = AIN2 = 5 V	mA max
Supply Current from V_{DD}	I_{DD}	−1, 2	7	7	7		$\overline{CS}$ = $\overline{RD}$ = V_{DD} AIN1 = AIN2 = 5 V	mA max

NOTES
[1]V_{DD} = +5 V ± 5%, V_{SS} = −12 V ± 10%, V_{REF} = −5V ± 1%.
[2]Order AD7672T(X)05/883B or AD7672T(X)10/883B.

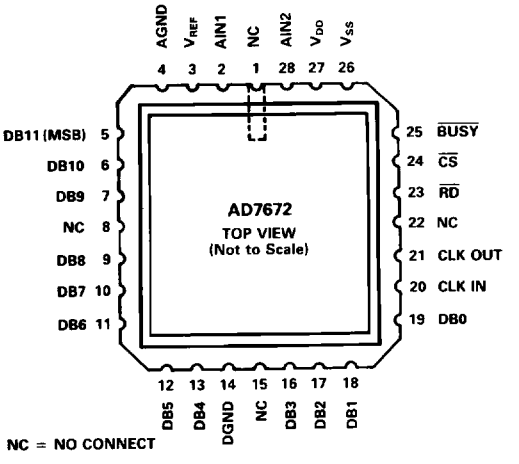
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

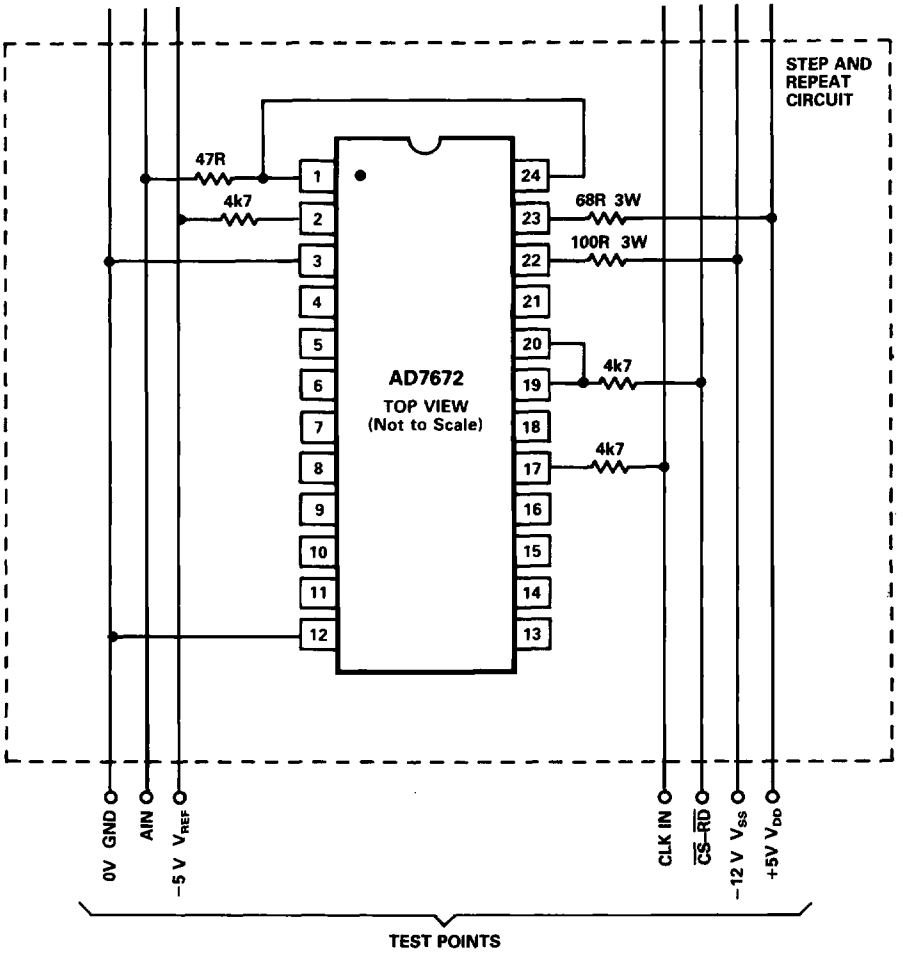


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by Technology Group (81).

4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7672 Burn-In

Power Supplies	Max Current
V_{DD} = +5 V	I_{DD} = 7 mA
V_{SS} = −12 V	I_{SS} = 12 mA
V_{REF} = −5 V	AIN = 3.5 mA

Input Logic Levels are 0 to +5 V.

1. *Static Burn-In*

   AIN is tied to ground.
   CLK IN Frequency is 35 kHz.
   After power up $\overline{CS}$–$\overline{RD}$ is taken high for 10 secs and is then taken low.
   CLK IN is then removed and tied high.

2. *Dynamic Burn-In*

   CLK IN is 100 kHz.
   AIN is driven with a 10 Hz sine wave input.
   $\overline{CS}$–$\overline{RD}$ is driven with a 160 μs period.
   AIN peak voltage 5 V.

   Power Up Sequence

   (1) V_{DD}
   (2) V_{SS}
   (3) V_{REF}
   (4) Inputs

AD7672 Burn-In Philosophy

Static Burn-In

1. After power-up the device performs a conversion on $\overline{CS}$–$\overline{RD}$ going low.
2. With AIN = 0 V and $\overline{CS}$–$\overline{RD}$ held low after the conversion, the digital outputs will be at 0 volts ensuring that the o/p n-channels will be put under maximum stress for the period of burn-in.
3. At the end of conversion with AIN = 0 V, little or no differential stress will exist between the input devices of the comparator.

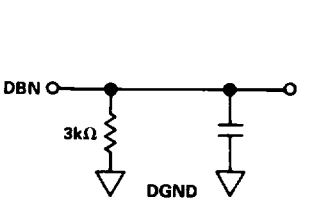
Dynamic Burn-In

CS–RD is brought low every 160 μs to start a new conversion and to ensure that the previous conversion has been completed.

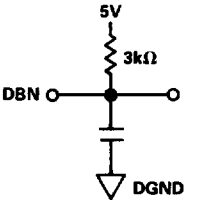
AD7672 TIMING[1] SPECIFICATIONS

Test	Symbol	Device	Design Limit T_{min} to T_{max}	Units
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1	−1, 2	0	ns min
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2	−1, 2	270	ns max
Data Access Time after $\overline{RD}$, C_L = 100 pF	t_3[2]		170	ns max
$\overline{RD}$ Pulse Width	t_4	−1, 2	t_3	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5	−1, 2	0	ns min
Data Setup Time after $\overline{BUSY}$	t_6[2]	−1, 2	100	ns max
Bus Relinquish Time	t_7[3]	−1, 2	20	ns min
			90	ns max
Delay Between Successive Read Operations	t_8	−1, 2	200	ns min

NOTES
[1]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

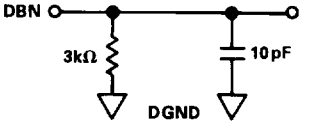


a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

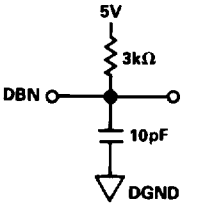


b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

6.0 Control Inputs Synchronization.

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT. This ensures a fixed conversion time that is 12.5 times the CLK IN frequency.

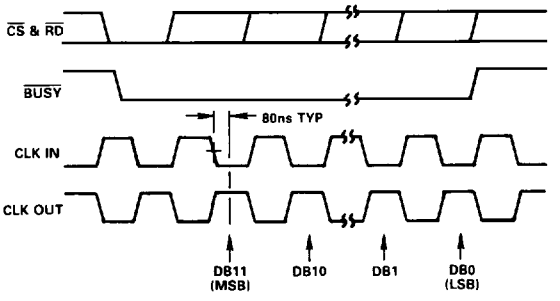


Figure 3. Operating Waveforms Using an External Clock Source for CLK IN

6.1 Driving the Analog Inputs.

During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4 MHz when CLK IN = 4 MHz). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample-and-hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically 11 mV with a 200 ns settling time.

Suitable devices capable of driving the AD7672 AIN input are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

6.2 Analog Input Ranges.

The AD7672 provides three user selectable analog input ranges: 0 to +5 V, 0 to +10 V and ±5 V. Figure 4 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

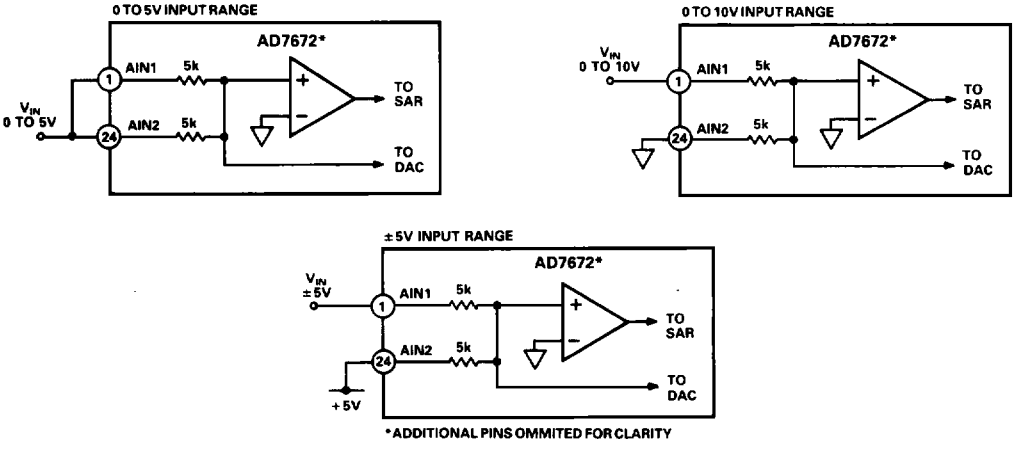


Figure 4. Analog Input Range Configurations

6.3 Unipolar Operation.

Figure 5 shows how to configure an AD584 to produce a reference voltage of −5 V for unipolar operation.

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, . . . FS −3/2 LSBs).

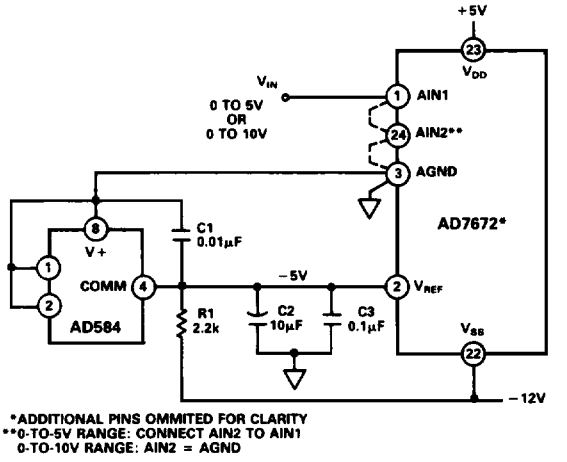


Figure 5. Unipolar Operation Using the AD584 as a Reference

6.4 Bipolar Operation.

Bipolar operation is achieved by providing a +10 V span at the AIN1 input which is offset to ±5 V by applying +5 V at the AIN2 input. This requires two reference voltages, −5 V for the V_{REF} input and +5 V for the AIN2 input. Figure 6 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. This device generates the required ±5 V with a minimum of additional components. It is also offers excellent temperature stability with voltage drifts as low as 1.5 ppm/°C.

The LSB size is (10/4096) V = 2.44 mV.

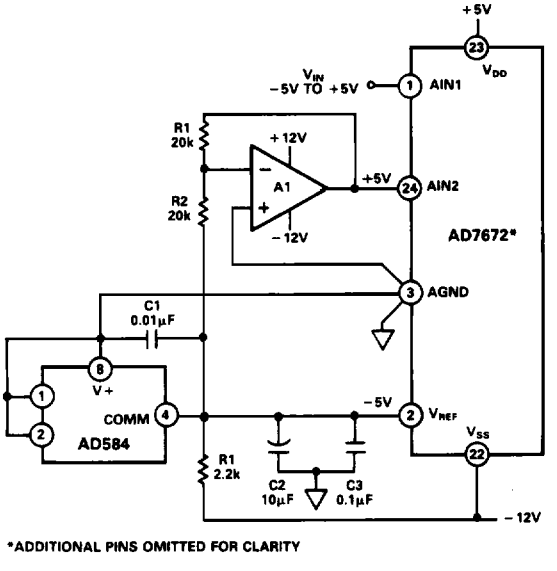


Figure 6. Bipolar Operation Using an AD584 and an AD711 Op Amp